Remarks

Election/ Restriction

Applicant thanks the examiner for his careful examination of the application. Through and oversight, an old set of claims was inadvertently referred to in responding to the election requirement.

Applicant agrees with the examiner's observation that the Fig. 7 embodiment does not include an additional highly doped region in the tub. Accordingly, applicant cancels claims 2, 10, 14 and dependent claims 6, 11, 12, 16, 17.
However, the dependent claims 3, 4, 5, 7, 8 are amended to depend from claim 1.

Applicant also agrees that claims 19 and 22 relate to the non-elected species and therefore cancels these claims as well as dependent claims 20 and 23.

Accordingly, the claims remaining in the application are claims 1, 9, 13, 15, 18, 21, 24, as identified by the examiner, as well as the amended claims 3, 4, 5, 7, 8.

Specification:
Please correct Page 2, line 18 in the "Field of the Invention" section by replacing "limited" with --limit--.
Please delete Page 1, line 19 in the "Field of the Invention" section by deleting "of the" after "One".
A clean copy of the "Field of the Invention" section is included.

Drawings
Figures 1-4 have been amended to include the legend "Prior Art". Red line and clean copies of the drawings are included.
Figure 3 is corrected by deleting the term "Top View". A red line and a clean copy of Figure 3 is included.
The examiner is thanked for noting the error.

Figure 3 has been corrected to include reference numeral 24. No new matter is added by the correction since page 2, line 1 clearly defines the region as the metal interconnect of the anode and because this region is clearly indicated in the plan view (Figure 2)

Figure 7 has been corrected to include reference numeral 254. No new matter is added by the correction since page 8, lines 14-16 clearly describes the location of the oxide regions 254.

Regarding Figures 5 and 6, applicant respectfully submits that the description for Figures 5 and 6 does not make reference to a substrate oxide. Insofar as the substrate is being referred to by the Examiner, this region is not shown in Figures 5 and 6, and therefore no label has been included. However, it was noted that the NBL 50 is not labeled in Figure 6. This has been corrected. No new matter has been added by this correction since the NBL is clearly described in Figure 6 by the legend "NBL".

Applicant has included new clean copies of Figures 5-7 and of the corrected drawing sheets. The corrections to Figures 6 and 7 were made on the new, more legible copies.

Claim Rejections – 35 USC 112
Claim 18 has been amended to make it clear that the first and second regions refer to the regions in the tub and that the reference to the polysilicon serves to indicate how the doped regions are formed in the tub.
A common way of forming doped regions (in the case of the Figure 7 embodiment, n-extrinsic base 262 and p+ region 266 formed in tub 250) is by forming doped poly regions on the device (in this case poly regions 260 and 264) and annealing to cause dopant to enter into the tub to form the regions 262, 266.
Claim 18 elaborates on this aspect by specifying that the dopant for the regions 262, 266 is obtained by two different poly layers as opposed to a single poly layer. For purposes of clarity, claim 18 has been amended to clarify this aspect. Similar amendments have been made to claims 5 and 8. No new matter is included by the amendment since support is found on page 8, lines 16-19. Also, this amendment was not made to overcome any prior art or for any other

reason related to patentability since these features were already inherent in the claim before amendment but have merely been emphasized for ease of understanding.

Claim Rejections – 35 USC 103

The embodiment of Figure 7 of the present application makes use of a unique structure that combines both NPN and PNP layers in providing a zener zap diode. Thus it allows conventional process steps in a double poly process to be used, and also achieves a zener diode that has the flexibility of providing different breakdown voltages, as is discussed below.

In contrast, Ibi merely makes use of a simple diode structure with anode 13 and cathode 14 formed in a p-type region 12. There is no teaching or suggestion of making use of double poly process steps in providing a zener zap diode.

As regards, Cervin, the device makes uses a traditional emitter-base configuration in which the emitter is formed in the base120 is formed in the base 124 as shown in Figure 10 and described in column 7, lines 13-15. This is where the shorting happens in Cervin. Thus it is limited to emitter-base breakdown of the transistor, which, once it is set, is fixed.

In contrast, the present application makes use of a collector-emitter junction to provide the breakdown junction. In this case the collector is defined by the tub which comprises n-epi or n-sinker 250 of a NPN transistor structure. The emitter is defined by p+ region 266 of a PNP transistor structure. Thus, in this configuration the p+ emitter 266 and base 262 of a PNP transistor structure are sitting in the NPN collector and are separated from each other instead of having the emitter formed in the base as in the Cervin structure. This structure of the present application provides the flexibility of having different breakdown voltages since the breakdown is across the collector-emitter junction. Claim 24 simply defines a structure in which the polarities are reversed.

Neither Cervin nor Ibi provide such a breakdown junction between collector and emitter and therefore do not provide adjustable breakdown voltages as is possible with the present embodiment. The independent claims 1, 9, 13, and 21 have been amended to emphasize the fact that the breakdown junction in the present application is between collector and emitter.

Thus none of the references teach or suggest using a standard double poly process to define a collector-emitter breakdown junction. In view of the differences between the present application and the prior art references, it is respectfully submitted that the present application is distinguishable over the prior art and in a position for allowance. The examiner is therefore respectfully requested to permit the claims remaining in the application to proceed to allowance.

Version with markings to show changes made:

1. (Amended) A zener zap diode device comprising

a p-doped emitter region formed in a n-type tub defining a collector,

a n-doped region formed in the tub and (that is) spaced from the p-doped emitter region, thereby defining a p-n junction between the p-doped emitter region and the tub or between the n-doped region and the tub depending on the doping of the tub,

and

a refractory metal silicide extending over part of at least the p-doped region, wherein the configuration of the device is such that the refractory metal silicide will form a silicide bridge across the p-n junction when a fusing current is established across the junction.

3. (Amended) A device of claim (2) 1, wherein the refractory metal silicide is Cobalt silicide.

4. (Amended) A device of claim (2) 1, wherein the silicide bridge is formed to extend between the silicide on the p-doped region and the silicide on the n-doped region or, if there is no silicide on the n-doped region, to a contact on the n-doped region.

5. (Amended) A device of claim (2) 1, wherein the dopant of the p-doped region is obtained from (formed by) a p-doped polysilicon layer and the dopant of the n-doped region is obtained from (formed by) a n-doped polysilicon layer, and the p-doped polysilicon layer and n-doped polysilicon layer are part of two different polysilicon layers in a multi-poly process.

7. (Amended) A device of Claim (2) 1, wherein the configuration of the device is such that the distance across which the bridge has to be formed is sufficiently short and the resistance path across which the bridge has to be formed is sufficiently low so as to allow the fusing current to be sufficiently low to avoid undesirable damage to the device when the fusing current is established across the junction.

8. (Amended) A device of claim (2) 1, wherein the dopant of the p-doped region is obtained from (formed by) a p-doped polysilicon layer and the dopant of the n-doped region is obtained from (formed by) a n-doped polysilicon layer, and wherein said n-doped polysilicon layer and p-doped polysilicon layer are spaced from each other by at least a nitride spacer.18.

(Amended) A device of claim 13, wherein the dopant of the first and second regions is obtained from doped polysilicon regions wherein the polysilicon regions are formed by two different poly layers in a double poly process.

9. (Amended) A zener zap diode device comprising

a p-doped emitter region formed in a n-type tub defining a collector,

a n-doped region formed in the tub that is spaced from the p-doped emitter region, thereby defining a p-n junction between the p-doped emitter region and the tub or between the n-doped region and the tub depending on the doping of the tub,

a refractory metal silicide extending across the junction.

13. (Amended) A zener zap diode device, comprising

an emitter (a first) region of a first polarity in a collector (tub) of opposite polarity to define a p-n junction,

a base (second) region with the same polarity as the collector (tub), spaced from the emitter (first) region, and

refractory metal silicide material in electrical contact with the emitter (first) and base (second) regions, wherein the configuration of the device is such that the refractory metal silicide will form a silicide bridge across the p-n junction when a fusing current is established across the junction.

18. (Amended) A device of claim 13, wherein the first and second regions are formed in the tub and the dopant of the first and second regions is obtained from (are formed by) two different poly layers in a double poly process.

21. (Amended) A method of forming a zener zap diode device, comprising

forming a first polysilicon layer on a n-type silicon,

n-doping the first polysilicon layer to form a n-base in the n-type silicon,

forming a second polysilicon layer on the n-type silicon, spaced from the first polysilicon layer,

p-doping the second polysilicon layer to form p+ emitter in the n-type silicon, spaced from the n-base,

depositing a refractory metal layer on at least part of the second polysilicon layer,

reacting the refractory metal with silicon to form a silicide, and

establishing a current between the first and second polysilicon layers to create a silicided bridge formed from the metal silicide to form a low resistance path between contacts to the first and second polysilicon layers, wherein the steps are performed in an order suitable for a double poly process.

24. (Amended) A method of forming a zener zap diode device, comprising

forming a first polysilicon layer on a p-type silicon,

p-doping the first polysilicon layer to form a p-base in the p-type silicon,

forming a second polysilicon layer on the p-type silicon, spaced from the first polysilicon layer,

n-doping the second polysilicon layer to form a n+ emitter in the p-type silicon, spaced from the p-base,

depositing a refractory metal layer on at least part of the first polysilicon layer,

reacting the refractory metal with silicon to form a silicide, and

establishing a current between the first and second polysilicon layers to create a silicided bridge formed from the metal silicide to form a low resistance path between contacts to the first and second polysilicon layers, wherein the steps are performed in an order suitable for a double poly process.

Respectfully Submitted,

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Field of the Invention

The accuracy of analog integrated circuits is typically limited by the amount of control one has during the fabrication process over the absolute value and matching tolerances of the integrated devices. This is particularly true in the case of mixed signal VLSI in which both digital and analog circuits are present, but the yield is largely limited by the analog circuit. Furthermore, in mixed signal integrated circuits, the digital circuits determine most of the size of the device, thus the failure of a small analog section of a chip has drastic implications on the yield of the mixed signal design.

Trimming techniques have been developed to improve the accuracy and yield of integrated circuits. Trimming refers to the making of adjustments to the integrated circuit after its fabrication is complete.

One trimming method is the use of anti-fuse approach applicable to both bipolar and CMOS designs. The term anti-fuse is used to describe an element which initially appears as an open-circuit but can be made to approach a short circuit by forcing conduction of a high-current for a short duration of time. Anti-fuse devices have been created in integrated circuits by various methods. One method creates anti-fuse devices by forcing a temporary avalanche breakdown in a p-n junction, sufficient to cause localized heating and subsequent migration of metal across the junction. This method of creating an anti-fuse is commonly referred to as zener zap.

Figure 1 shows a typical application of zener zap diodes to achieve resistor trimming. Diodes 10 are connected in parallel with resistors 12 wherein each of the resistors 12 is made small compared to the total resistance of the resistor string. Pads 14 allow each of the individual zener zap diodes 10 to be contacted to apply the requisite current to convert the effective open circuit of the diode 10 to a short circuit. Commonly, zener zap diodes are created as illustrated in Figure 2, with the cathode of the diode created as a circular diffusion with a contact 20. The cathode is typically heavily doped n-material, which may be 1-3 microns deep with sheet resistance of 5-10 Ohms per square. In contrast, the anode 22 is created by a moderately doped p-diffusion, for example, 3-5 microns deep with sheet resistance of 100-200 Ohms per square.

The metal interconnect 24 of the anode 22 presents a flat surface to the contact of the cathode 20. In this embodiment, the n+diffusion is placed inside the p-diffusion as in a

conventional bipolar transistor device. This is also illustrated in a cross-section in Figure 3 showing the cathode 20 in the anode 22. It will, however, be appreciated that other configurations may be used such as the one illustrated in Figure 4. In this embodiment, the cathode 40 forms only a small overlap with the p diffusion of the anode 42.

It has been shown that for a diode doped as discussed with reference to Figures 2 and 3, where the n-material is heavily doped and the p-diffusion is only moderately doped, the p-material doping will determine the junction breakdown. The higher the doping of the p-material, the lower the breakdown voltage. Furthermore, since most fabrication processing creates a doping profile that results in maximum density at the surface of the doped material, the voltage breakdown typically occurs at the surface of the vertical p-n junction.

At breakdown, power is dissipated in the junction as given by the equation

$$P = BV.I$$

where I is the current conducted through the junction during breakdown, BV is the breakdown voltage, and P is the power dissipated in the junction. If no limit is placed on current I, the junction will heat rapidly and can destroy a number of mechanisms. On the other hand, if current I is limited, the power P will cause localized heating around the area where the current is concentrated. If current I is applied for a fixed time, sufficient heating can occur to cause migration of atoms of the metal interconnection from the cathode terminal to the anode terminal of the diode along the path of the breakdown current. This migration of metal establishes a trace of metal, typically aluminum, embedded in the silicon along the path of the current, near the surface. This electro migration of aluminum comprises two phases. During the first phase an initial breakdown and heating occurs during which the metal interconnect atoms are mobilized and begin to flow across the junction. The second phase involves the carrying of a sufficient number of the metal atoms to create a low resistance path through the silicon. One approach found to work well is to initiate the first phase with a high peak current of short duration, followed by a lower current of longer duration. For example, a current of 100-200 mA may be applied for 0.5-1 milliseconds followed by a current of 30-60 mA for a period of 2-3 milliseconds. Once the metal has migrated and created a current path, the zener zap diode is essentially short circuited. Thus, in a cascaded resistor network as illustrated in Figure 1, the zener zap diodes 10 can be selectively short circuited by applying the appropriate high current to the pads 14.

As integrated circuits become ever smaller and bearing in mind the risk of electrostatic discharge (ESD) currents, the aluminum contacts pose the risk of unwanted migrations taking place in certain integrated circuit devices. As a result, aluminum contacts have been isolated from the silicon using tungsten plugs. By introducing the creation of tungsten plugs in the process, the migration of aluminum in zener zap diodes is, however, also prevented. What is needed is a way of producing a zener zap anti-fuse while dealing with the fact that the aluminum needs to be isolated from the silicon, for example, by the use of tungsten plugs.